

CLAIMS

What is claimed is:

- 1 1. A content addressable memory (CAM) apparatus comprising:
2 an array of CAM cells;
3 a select circuit adapted to generate a plurality of select signals each indicative of a
4 segment of input data provided to the CAM apparatus; and
5 switch circuitry including a plurality of programmable switch circuits each
6 programmable to output a respective bit of the input data as a comparand bit for the array
7 of CAM cells in response to one of the select signals.
- 1 2. The CAM apparatus of claim 1, wherein the select circuit comprises:
2 a memory storage circuit for storing programmed segment information; and
3 a compare circuit coupled to the memory storage circuit to compare the
4 programmed segment information with input segment information to generate one of the
5 select signals.
- 1 3. The CAM apparatus of claim 2, wherein the compare circuit and the memory
2 storage element form a CAM cell.
- 1 4. The CAM apparatus of claim 1, wherein the switch circuitry comprises a cross-
2 bar switch.

1 5. The CAM apparatus of claim 1, wherein the switch circuitry comprises L rows of
2 L programmable switch circuits coupled to receive L input bits of the input data and L
3 select signals from the select circuit.

1 6. The CAM apparatus of claim 5, wherein the L inputs bits are one of N segments
2 of M input bits where M is equal to N multiplied by L.

1 7. The CAM apparatus of claim 1, further comprising a comparand storage element
2 coupled between the plurality of programmable switch circuits and the array of CAM
3 cells, the comparand storage element to store the comparand input bit.

1 8. The CAM apparatus of claim 7, further comprising a global mask register coupled
2 between the comparand storage element and the array of CAM cells.

1 9. The CAM apparatus of claim 1, further comprising a program circuit coupled to
2 the switch circuits to program the plurality of programmable switch circuits.

1 10. The CAM apparatus of claim 1, wherein the input bit has a first bit position in an
2 input data and the comparand bit has a second, different bit position in comparand data
3 for the array of CAM cells.

1 11. A content addressable memory (CAM) apparatus comprising:
2 an array of CAM cells;

3 means for generating a plurality of select signals each indicative of a segment of
4 input data provided to the CAM apparatus; and
5 switch circuitry including a plurality of programmable switch circuits each
6 programmable to output a respective bit of the input data as a comparand bit for the array
7 of CAM cells in response to one of the select signals.

1 12. The CAM apparatus of claim 11, wherein the switch circuitry comprises a cross-
2 bar switch.

1 13. A content addressable memory (CAM) apparatus comprising:
2 X CAM array blocks each having R rows of L CAM cells, where X, R, and L are
3 integers greater than one and wherein the CAM apparatus has a total of R multiplied by X
4 rows of CAM cells;

5 X select circuits each adapted to generate a plurality of select signals each
6 indicative of a segment of input data provided to the CAM apparatus; and

7 X switch circuits each including a plurality of programmable switch circuits each
8 programmable to output a respective bit of the input data as a comparand bit for a
9 corresponding one of the CAM array blocks in response to one of the select signals.

1 14. The CAM device of claim 13, wherein at least one of the select circuits
2 comprises:

3 a memory storage circuit for storing programmed segment information; and

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4 a compare circuit coupled to the memory storage circuit to compare the
5 programmed segment information with input segment information to generate one of the
6 select signals.

1 15. The CAM apparatus of claim 14, wherein the compare circuit and the memory
2 storage element form a CAM cell.

1 16. The CAM apparatus of claim 13, wherein at least one of the switch circuits
2 comprises a cross-bar switch.

1 17. The CAM apparatus of claim 13, wherein at least one of the switch circuits
2 comprises L rows of L programmable switch circuits coupled to receive L input bits of
3 the input data and L select signals from the corresponding select circuit.

1 18. The CAM apparatus of claim 17, wherein the L inputs bits are one of N segments
2 of M input bits where M is equal to N multiplied by L.

1 19. The CAM apparatus of claim 13, further comprising at least one program circuit
2 coupled to at least one of the switch circuits to program the plurality of programmable
3 switch circuits.

1 20. The CAM apparatus of claim 13, wherein the input bit has a first bit position in an
2 input data and the comparand bit has a second, different bit position in comparand data.

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1 21. A content addressable memory (CAM) apparatus comprising:
 2 an array of CAM cells having Z rows of X segments of L CAM cells, where X, Z,
 3 and L are integers greater than one and wherein the CAM apparatus has a total of Z rows
 4 of CAM cells;

5 X select circuits each adapted to generate a plurality of select signals each
 6 indicative of a segment of input data provided to the CAM apparatus; and

7 X switch circuits each including a plurality of programmable switch circuits each
 8 programmable to output a respective bit of the input data as a comparand bit for a
 9 corresponding one of the CAM array blocks in response to one of the select signals.

1 22. The CAM device of claim 21, wherein at least one of the select circuits
 2 comprises:

3 a memory storage circuit for storing programmed segment information; and
 4 a compare circuit coupled to the memory storage circuit to compare the
 5 programmed segment information with input segment information to generate one of the
 6 select signals.

1 23. The CAM apparatus of claim 22, wherein the compare circuit and the memory
 2 storage element form a CAM cell.

1 24. The CAM apparatus of claim 21, wherein at least one of the switch circuits
 2 comprises a cross-bar switch.

1 25. The CAM apparatus of claim 21, wherein at least one of the switch circuits
2 comprises L rows of L programmable switch circuits coupled to receive L input bits of
3 the input data and L select signals from the corresponding select circuit.

1 26. The CAM apparatus of claim 25, wherein the L inputs bits are one of N segments
2 of M input bits where M is equal to N multiplied by L.

1 27. The CAM apparatus of claim 21, further comprising at least one program circuit
2 coupled to at least one of the switch circuits to program the plurality of programmable
3 switch circuits.

1 28. The CAM apparatus of claim 21, wherein the input bit has a first bit position in an
2 input data and the comparand bit has a second, different bit position in comparand data.

1 29. A method comprising:
2 programming a select circuit to generate a plurality of select signals each
3 indicative of a segment of input data provided to a content addressable memory (CAM)
4 apparatus having an array of CAM cells; and
5 programming switch circuitry to output a respective bit of the input data as a
6 comparand bit for the array of CAM cells in response to one of the select signals.

1 30. A method comprising:
 2 receiving a plurality of segments of input data in a content addressable memory
 3 (CAM) apparatus having an array of CAM cells;
 4 receiving segment information indicative of which segment of the input data is
 5 received at any given time; and
 6 selectively enabling, in response to the segment information, programmed switch
 7 circuitry to filter at least one bit of the input data to generate at least one comparand bit
 8 for the array of CAM cells.

1 31. The method of claim 30, wherein the selectively enabling further comprises
 2 selectively enabling at least one programmed switch circuit to couple one bit of the input
 3 data to at least one bit position of a comparand storage element.

1 32. The method of claim 30, further comprising comparing the comparand bit with
 2 data stored in the array of CAM cells.